



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,136	02/26/2004	Naoki Ito	01-560	3489

23400 7590 08/10/2007
POSZ LAW GROUP, PLC
12040 SOUTH LAKES DRIVE
SUITE 101
RESTON, VA 20191

EXAMINER

JANAKIRAMAN, NITHYA

ART UNIT	PAPER NUMBER
----------	--------------

2123

MAIL DATE	DELIVERY MODE
-----------	---------------

08/10/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/786,136	Applicant(s) ITO ET AL.	
	Examiner Nithya Janakiraman	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 2/26/04.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
- ☒ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>2/26/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This action is in response to the application filed on 2/26/2004. Claims 1-16 are presented for examination.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on February 28, 2003. It is noted, however, that applicant has not filed a certified copy of the foreign priority application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,877,112, Iino (hereinafter Iino).

3. Regarding claim 1 (and 9), Iino discloses:

A semiconductor integrated circuit device for emulating operation of a one-chip microcomputer having a CPU and a peripheral circuit that is controlled by the CPU (see Figure 4, "Emulator"), the device comprising:

Art Unit: 2123

a vector address switching circuit for outputting a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal, and for outputting a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal (see column 2, lines 55-67, column 3, lines 1-6); and

an interface circuit for performing input and output of information relating to emulation between the CPU and an external circuit (see column 2, lines 31-35),

wherein the CPU is constructed to be reset by the first and second reset signals and the interface circuit is constructed to be reset by the second reset signal (see Figure 4: **13, 21**).

4. Regarding claim 2 (and 10), Iino discloses:

The semiconductor integrated circuit device according to claim 1, wherein:

the peripheral circuit includes a functional circuit for realizing a primary function of the peripheral circuit, a stop control circuit for stopping, in response to reception, by the CPU, of a break request that has occurred during execution of an instruction by the CPU, progress of an operation of the functional circuit until completion of processing that is performed in response to the break request, and a setting information storage circuit for storing setting information indicating whether to enable or disable an operation stop function of the stop control circuit (see column 1, lines 28-39); and

the functional circuit of the peripheral circuit is constructed to be reset by the first and second reset signals, and the stop control circuit and the setting information storage circuit are

constructed to be reset by the second reset signal (see column 2, lines 55-67, column 3, lines 1-6).

5. Regarding claim 3 (and 11), Iino discloses:

The semiconductor integrated circuit device according to claim 1, further comprising:
an emulation memory for storing a user program (see column 2, lines 10-20); and
a monitor program memory for storing a monitor program (see column 1, lines 21-27).

6. Regarding claim 4 (and 12), Iino discloses:

The semiconductor integrated circuit device according to claim 1, wherein:
the CPU is operable in an normal operation mode and a low power consumption operation mode that is lower in power consumption than the normal operation mode (see column 1, lines 40-45);
and
a break request control circuit is provided for causing a transition of the CPU to a break state after input of a wake-up signal for returning the CPU from the low power consumption operation mode to the normal operation mode when a break request signal is input externally in a period when the CPU is in the low power consumption operation mode (see column 1, lines 28-39).

7. Regarding claim 5 (and 13), Iino discloses:

The semiconductor integrated circuit device according to claim 4, wherein the break request control circuit is constructed to immediately output a break request signal to the CPU if the break

Art Unit: 2123

request signal is input in a period when the CPU is in the normal operation mode, and outputs a break request signals to the CPU upon input of the wake-up signal if the break request signal is input in a period when the CPU is in the low power consumption operation mode (see column 1, lines 28-45).

8. Regarding claim 6 (and 14), Iino discloses:

The semiconductor integrated circuit device according to claim 4, further comprising:
a break request control register that is reset by the second reset signal (see column 2, lines 55-63),

wherein the break request control circuit is constructed to cause a transition of the CPU to the break state immediately or after input of the wake-up signal when the break request signal is input externally in a period when the CPU is in the low power consumption operation mode depending on a value of the break request control register (see column 1, lines 28-39).

9. Regarding claim 7 (and 15), Iino discloses:

The semiconductor integrated circuit device according to claim 4, further comprising:
a wake-up signal generation circuit for generating a wake-up signal when a prescribed set time has elapsed from a transition of the CPU from the normal operation mode to the low power consumption operation mode (see column 1, lines 40-45).

10. Regarding claim 8 (and 16), Iino discloses:

Art Unit: 2123

The semiconductor integrated circuit device according to claim 7, wherein the wake-up signal generation circuit includes:

a counter for performing a counting operation in a period when the CPU is in the low power consumption operation mode (see column 9, line 61);

a storage circuit for storing a set count corresponding to the set time (see column 2, line 18); and

a comparator circuit for comparing a value of the counter with the set count of the storage circuit, and for outputting the wake-up signal when the value of the counter has reached the set count (see column 10, lines 3-14).

Additional References

11. US Patent 6,704,895: An emulation device including a serial scan testability interface having at least first and second scan paths, and state machine circuitry connected and responsive to said second scan path generally operable for emulation control.

Conclusion

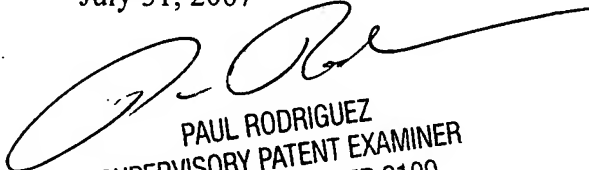
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nithya Janakiraman whose telephone number is 571-270-1003. The examiner can normally be reached on Monday-Thursday, 8:00am-5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on (571)272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nithya Janakiraman
Art Unit 2123
July 31, 2007

NJ


PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100